



**SDI FINAL EVALUATION FORM 1.1**

**PART 1:**

|                          |                                                                      |
|--------------------------|----------------------------------------------------------------------|
| Journal Name:            | <a href="#">British Journal of Applied Science &amp; Technology</a>  |
| Manuscript Number:       | 2014_BJAST_10586                                                     |
| Title of the Manuscript: | CARBON NANO TUBE FIELD EFFECT TRANSISTOR BASED 4-BIT FULL ADDER CELL |

**PART 2:**

| FINAL EVALUATOR'S comments on revised paper (if any)                                                                                                                                                                                                                                                                | Authors' response to final evaluator's comments                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>Author should clarify the difference and comparison with the below literature.<br/>           Mirzaee R F, Moaiyeri M H, Maleknejad M, et al. Dramatically low-transistor-count high-speed ternary adders[C]//Multiple-Valued Logic (ISMVL), 2013 IEEE 43rd International Symposium on. IEEE, 2013: 170-175.</p> | <p>I have compared the 4-bit adder proposed by me with the paper mailed by you.<br/>           First of all, in that paper the results for 4-bit full adder are not mentioned in detail.<br/>           I have found that if we design the 4- bit adder using the 1-bit adder mentioned by them; number of transistors used is very large.<br/>           When the power consumption of both the adders is compared then for the proposed adder it is much better then the power consumed by ternary 1-bit adder.<br/>           So, this may affect the overall power delay product of 4-bit adder.</p> |