

Dramatically Low-Transistor-Count High-Speed Ternary Adders

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Abstract—Ternary logic has inherently the potential of high computational speed in comparison with conventional binary logic. A new low-transistor-count, high-speed ternary half adder is presented in this paper. Carbon nanotube field effect transistors are utilized to realize the new design methodology. Unique characteristics of this technology provide multi- V_t circuitry with the flexibility which is highly essential for MVL designs. The given structure also benefits from high driving power and capability of operating in low voltages. It has only 26 transistors. A new high-performance ternary full adder is also presented. Finally, the proposed adder cells are put together in order to construct a 4-bit ternary ripple adder.

Keywords—ternary half adder, ternary full adder, CNTFET, 4-bit ternary ripple adder, high-speed, nanoelectronics

I. INTRODUCTION

Binary logic has mainly been the dominant logic among VLSI designers over the past few decades due to the intrinsic switching behavior of a transistor. The on-off states of a transistor make it an ideal device to implement Boolean algebra. However, dealing with real-world applications is the Achilles' heel of dualism. This is the point where Multiple-Valued Logic (MVL) surpasses. In addition, MVL circuitry has the advantages of less product cost and complexity, fewer on-chip/off-chip interconnections, and higher computational power due to the fact that more information can be transmitted and stored in a fixed memory length [1]. Among many MVL systems, ternary logic is the most efficient [2].

To put large ternary systems in practice, high-efficient ternary gates need to be first realized. Adder is one of the most important blocks. It plays an important role in many VLSI applications [3], and it lies on the critical path of almost all arithmetic systems. Therefore, higher efficiency of the adder block affects total enhancement of the whole system.

Ternary logic is based on an additional voltage level. Therefore, flexibility in designing multi- V_t circuits is highly desired. Carbon Nanotube Field Effect Transistor (CNTFET) is a recently noted technology which is highly appropriate for multi- V_t circuitry. The ability of adjusting desired threshold voltage by simply altering the diameter of CNTs is the key

factor in this domain [4]. In addition, CNTFET is the most well-known successor to traditional MOSFET technology because of their similarities regarding intrinsic characteristics, and the existence of both n-type and p-type transistors.

A gate-level design of a Ternary Half Adder (THA) has been proposed in [5], which uses basic ternary gates to form the adder block. The main drawback is high number of transistors, which is in contrast with initial MVL targets. A modified version of the previous half adder has been presented in [6], with the aim of reducing transistor count. It replaces ternary ANDs and three ternary ORs with the binary ones. The third attempt is a high-performance NAND-based structure which has been presented in [7]. New decoders and new ternary NANDs have been utilized in order to enhance delay and power consumption factors. Although it benefits from high

efficiency, it still requires 112 transistors. Moreover, a $\frac{V_{dd}}{2}$

voltage reference is also required. Extra interconnections are needed in case of adding another power supply to the circuit. Having multiple on-chip voltages brings additional physical constraints in terms of placement and routing [8].

A ternary full adder cell has been also presented in [9]. It is on the basis of cascading two pseudo-half adder blocks to create Sum. The so-called half adder does not produce C_{out} . The final output carry is generated by another sub-circuit. It has 106 transistors including ternary inverters which produce complementary input signals. In spite of full-swing operation, it suffers from low driving power due to its long critical path consisting of several pass-transistors in series.

In this paper, a dramatically low-transistor-count, high-performance ternary half adder is presented. Resistors and capacitors are utilized as voltage dividers in this paper. Both elements are implemented with the usage of transistors. The designing process to reach a final structure is presented through four steps. High speed, high driving power, and capability of working in low voltages are the main advantages of the proposed design. A new Ternary Full Adder (TFA), which is another essential component of addition, is also presented. Eventually, both adder blocks are employed to realize a 4-bit ternary ripple adder block.

The rest of the paper is organized as follows: Section 2 contains motivation. Section 3 illustrates how the novel ternary half adder is achieved. The new ternary full adder and ternary ripple adder are presented in section 4 and section 5, respectively. Finally, section 6 concludes the paper.

II. MOTIVATION

Ternary system of numeration consists of Ternary digITs (TITs). The $\{0, 1, 2\}_3$ set is the most common notation. Taking ternary logic into account, the output Sum can be calculated by Eq. 1. The second output of a ternary half adder, C_{out} , is equal to the addition of input arguments divided by three (Eq. 2). This is an integer division, which means the fractional part has to be discarded. The integer division is denoted by ' $\setminus$ '. The equations exhibit that both outputs (Sum and C_{out}) are reliant upon the sum of the input variables ($\Sigma_{in}=A+B$). This similarity is exploited in this paper in order to reach a novel design where circuit integration leads to a great reduction in the number of transistors. Two ternary inputs form nine different states. The truth table of a ternary half adder is shown in Table 1.

$$\text{Sum} = (A + B) \bmod 3 = \Sigma_{in} \bmod 3 \quad (1)$$

$$C_{out} = \lfloor \frac{A + B}{3} \rfloor = (A + B) \setminus 3 = \Sigma_{in} \setminus 3 \quad (2)$$

TABLE I. TRUTH TABLE OF A TERNARY HALF ADDER AND THE REQUIRED THRESHOLDS

Σ_{in}	Threshold (TH)	$\frac{\Sigma_{in}}{2}$	Switching Threshold (ST)	C_{out}	Sum
0		0		0	0
1	0.5	0.5	0.25	0	1
2	1.5	1	0.75	0	2
3	2.5	1.5	1.25	1	0
4	3.5	2	1.75	1	1

The highest boundary of Σ_{in} is four. It occurs when both operands equal logic value '2'. Starting from $\Sigma_{in}=0$, four distinctive increasing Thresholds (TH) are defined (Table 1), which are the average of two successive rows of the column Σ_{in} . Output functions (Sum and C_{out}) might have different logic values moving below and above a specific threshold. For instance, when Σ_{in} increases from 0 to 1, TH=0.5 is met and the output Sum switches from '0' to '1'.

The Σ_{in} parameter can simply be implemented by the usage of two capacitors (Fig. 1) in digital electronics. The capacitors perform voltage division between input signals (V_A and V_B),

and the result is $\frac{V_A + V_B}{2}$ (Eq. 3). Therefore, defined thresholds have to be also divided by two (Eq. 4). The half thresholds are identified by Switching Thresholds (ST) in Table 1. STs are in fact the average of two successive rows of the $\frac{\Sigma_{in}}{2}$ column. Finally, two distinctive threshold-sensitive circuits generate the proper outputs.

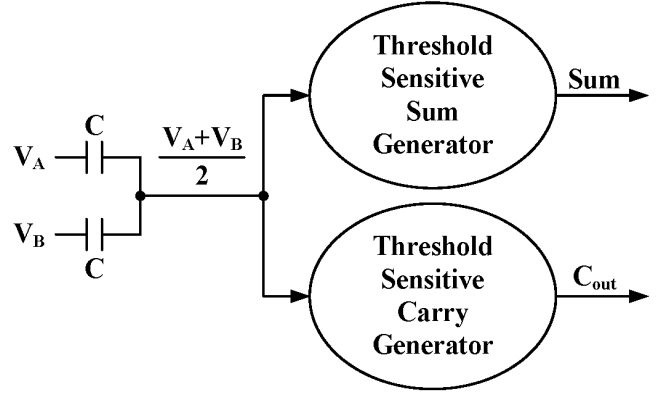


Figure 1. The preliminary schema of the proposed ternary half adder

$$\frac{V_A \times C + V_B \times C}{C + C} = \frac{V_A + V_B}{2} \quad (3)$$

$$ST = \frac{TH}{2} \quad (4)$$

III. THE PROPOSED HALF ADDER

The whole designing process is divided into four steps. The initial design will be modified progressively to reach a high-performance structure.

A. The Initial Design

The initial design (Fig. 2) implements both outputs directly. Each transistor is marked with the proper ST parameter, which determines whether the transistor is switched on or off. An n-type transistor whose gate terminal receives a voltage more than V_{ST} (Eq. 5), switches on. The same voltage level results in switching off a p-type transistor. As it is lucid, the threshold voltages of n-type and p-type transistors can be defined by Eq. 6 and Eq. 7, respectively. V_{ST} is actually the definition of the threshold voltage for an n-type transistor.

$$V_{ST} = \frac{ST \times V_{dd}}{2} \quad (5)$$

$$V_{th,n} = V_{ST} \quad (6)$$

$$|V_{th,p}| = V_{dd} - V_{ST} \quad (7)$$

Unlike an MOS device, which is inherently single-threshold [10], different threshold voltages are feasible to be achieved in a CNTFET device by simply altering the diameter of the nanotubes (D_{CNT}), laying under the gate terminal. This is a unique characteristic which makes CNTFET an ideal device to implement MVL circuits. The relationship between threshold voltage and D_{CNT} is shown in Eq. 8. Moreover, D_{CNT} is a function of chiral vectors (n_1, n_2) (Eq. 9) [11].

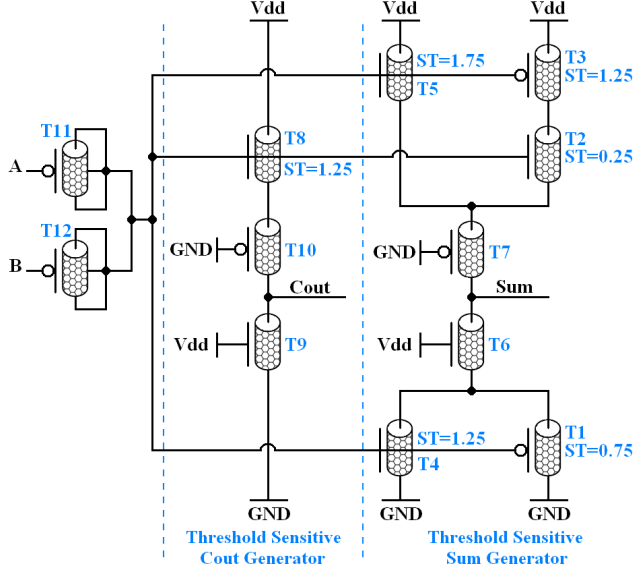


Figure 2. The proposed ternary half adder (Initial Design)

$$V_{th} \approx \frac{0.43}{D_{CNT} \text{ (nm)}} \quad (8)$$

$$D_{CNT} \text{ (nm)} \approx 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 \times n_2} \quad (9)$$

Table 2 summarizes how transistors connect the output node Sum to the appropriate voltage source (V_{dd} or GND).

When $\frac{\Sigma_{in}}{2} = 0$, the first transistor (T_1) is switched on. It connects the output node to the ground through the Pull-Down (PD) network. Although T_3 is also ON, the Pull-Up (PU) network is disconnected because T_2 , which is in series with T_3 , is OFF. When $\frac{\Sigma_{in}}{2} = 0.5$, T_2 also switches on and both PD and PU networks are subsequently on. T_6 and T_7 act as voltage dividers, and generate logic value '1'. As the value of Σ_{in} increases, the output node gets the proper value through new paths constructed by transistors in PD, PU, or both networks. The ON states of transistors causing the output node to have the proper value are distinguished in Table 2 (in bold/italic) from the ones which do not affect the output node.

TABLE II. SWITCHING ACTIVITY FOR SUM GENERATOR CIRCUIT (RELATED TO FIG. 2)

$\frac{\Sigma_{in}}{2}$	T_1	T_2	T_3	T_4	T_5	PD	PU	Sum
0	ON	OFF	ON	OFF	OFF	ON	OFF	0
0.5	ON	ON	ON	OFF	OFF	ON	ON	1
1	OFF	ON	ON	OFF	OFF	OFF	ON	2
1.5	OFF	ON	OFF	ON	OFF	ON	OFF	0
2	OFF	ON	OFF	ON	ON	ON	ON	1

The carry generator circuit operates in the same manner.

Whenever $\frac{\Sigma_{in}}{2}$ becomes more than $ST=1.25$ (Table 1), T_8

switches on and the output carry becomes '1'. Otherwise, C_{out} is only connected to the ground. T_9 and T_{10} are always switched on. They perform voltage division between pull-up and pull-down networks whenever the output node has to be '1'.

Referring to digital electronics, the voltage level of $\frac{V_{dd}}{2}$

represents logic value '1'. Passive electronic components such as resistors or capacitors could be utilized to perform voltage division in order to generate '1' [12]. Although the usage of capacitors as voltage dividers brings about less static power dissipation, the usage of resistors leads to higher driving power and circuit robustness. Resolving fabrication constraints, transistors themselves could be employed to implement both resistors and capacitors. A constantly switched-on transistor could function as a voltage divider. The n-type and the p-type CNTFETs with identical parameters bring about the same resistance due to the same mobility of N and P substances [13]. In order to obtain higher resistivity, channel, and doped CNT source- and drain-side extension regions for these transistors have been lengthened by 90nm. The number of nanotubes under the gate terminal has also been decreased (#CNTs=2).

Finally, T_{11} and T_{12} perform the initial voltage division. CNTFETs are again employed to implement capacitors [14]. One plate of CNTFET capacitor is the source-drain-substrate junction and the other plate is the gate terminal. The capacitance of a CNTFET capacitor is calculated by Eq. 10, where N is the number of nanotubes under the gate, C_{CNT} is the capacitance of one CNT, and C_{Gate} is the capacitance due to the gate size in CNTFET [14]. Both C_{Gate} and N parameters have been increased ($L_{ch}=180\text{nm}$ and #CNTs=500), so that higher capacitance is achieved.

$$C_{CNTFET} = N \times C_{CNT} + C_{Gate} \quad (10)$$

B. Adding Supplimentary Inverters

Due to the non-full-swing behavior of transistors, the n(p)-type transistors in the PU(PD) network have to be replaced with p(n)-type ones. Supplementary inverters are added to control the switching activity of the replaced transistors. The modified schema of the initial design with the usage of supplementary inverters is illustrated in Fig. 3. Both outputs are generated directly and the whole cell has 20 transistors. ST parameters are shifted from the pass transistors to the inverters, so that the entire circuit operates in accord with the initial design. The Voltage Transfer Characteristic (VTC) curves of the supplementary inverters are plotted in Fig. 4. After the replacement procedure, the whole cell complies with the standard CMOS circuitry, in which all pCNTFETs are located in the pull-up network, and all nCNTFETs are placed within the pull-down network.

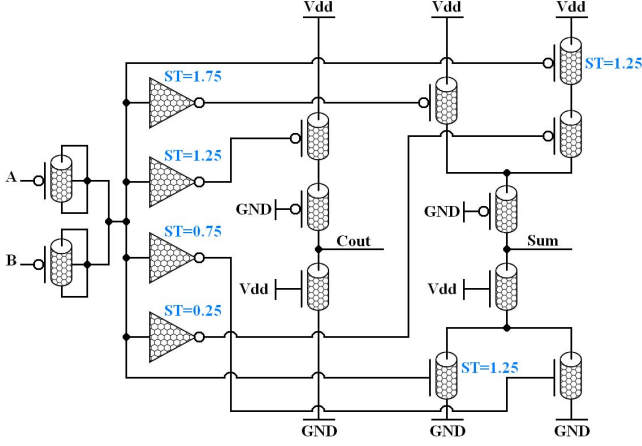


Figure 3. The proposed ternary half adder with the usage of supplementary inverters

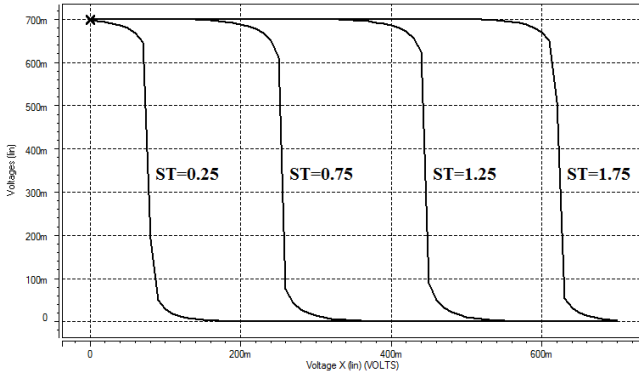


Figure 4. VTC curves of the supplementary inverters

C. Implementing Inverted Outputs (Indirect Approach)

To improve driving capability of the given structure, an indirect approach is taken into consideration as the third step of reaching a high-performance ternary half adder cell. Therefore, complementary outputs ($\overline{\text{Sum}}$ and $\overline{C_{\text{out}}}$) are first generated (Fig. 5) by using the same method which was described before. Then, two ternary inverters generate the non-inverted outputs (Sum and C_{out}). Not only does the final inverter result in higher driving power when facing long wires or high number of fan-outs, but it also isolates the internal nodes from any output loads. The switching activity of transistors is summarized in Table 3. The highlighted switched-on transistors link the output node to the proper voltage source.

TABLE III. SWITCHING ACTIVITY FOR $\overline{\text{Sum}}$ GENERATOR CIRCUIT (RELATED TO FIG. 5)

$\frac{\Sigma_{\text{in}}}{2}$	T ₁	T ₂	T ₃	T ₄	T ₅	PD	PU	$\overline{\text{Sum}}$
0	ON	OFF	ON	OFF	OFF	OFF	ON	2
0.5	ON	ON	ON	OFF	OFF	ON	ON	1
1	OFF	ON	ON	OFF	OFF	ON	OFF	0
1.5	OFF	ON	OFF	ON	OFF	OFF	ON	2
2	OFF	ON	OFF	ON	ON	ON	ON	1

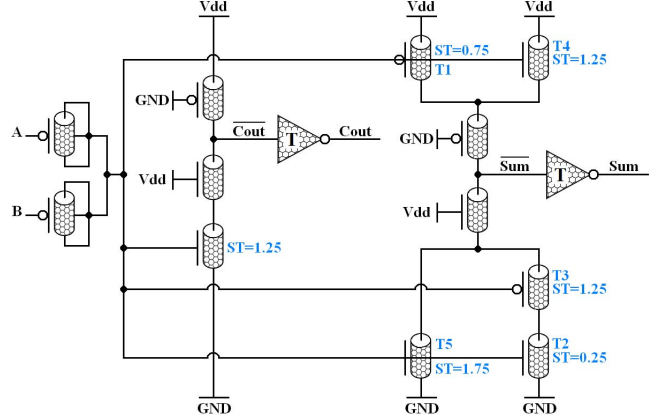


Figure 5. The proposed ternary half adder (Indirect Approach)

D. The Final Design

As mentioned before, pCNTFETs in the pull-down network (nCNTFETs in the pull-up network) have to be replaced with their counterparts. One supplementary inverter is adequate for the transistors with the same ST parameters. The final schema of the proposed ternary half adder is depicted in Fig. 6. It has only 26 transistors. Each transistor is marked with the number of CNTs (#CNTs) and their diameters. The Standard Ternary Inverter (STI) presented in [7] is used to generate Sum and C_{out} . The final inverters result in high driving power. The indirect approach has another great advantage. The node which is the result of initial voltage division between capacitors has to drive 10 transistors in the direct approach (Fig. 3). The indirect approach leads to a reduction in driving necessity for the same node. Since this node is not directly connected to neither of the voltage sources, the fewer fan-outs there are, the better performance it has. The same node has to drive six transistors in the final design (Fig. 6).

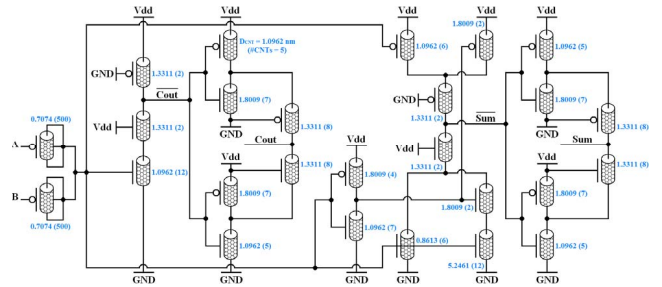


Figure 6. The proposed ternary half adder (Final Design)

E. Simulation Results

The proposed ternary half adder (Final Design) and the design presented in [7] are simulated by using Synopsys HSPICE simulator with the Compact SPICE Model for 32nm CNTFETs, including all nonidealities [15]. Presented ternary buffers in [7] together with 2fF load capacitors are used to provide a realistic simulation setup. All 72 transitions are fed to the circuits to achieve maximum cell delay. Simulations are repeated in three different power supply voltages (0.75V, 0.7V,

and 0.65V) at room temperature, and after performing transistor sizing. The average power consumption during all transitions is also reported. The Power-Delay Product (PDP) makes a trade-off between delay and power factors (Eq. 11). Finally, the waveforms of the proposed ternary half adder are also depicted in Fig. 7.

$$PDP = \text{Max}(\text{Delay}) \times \text{Avg}(\text{Power}) \quad (11)$$

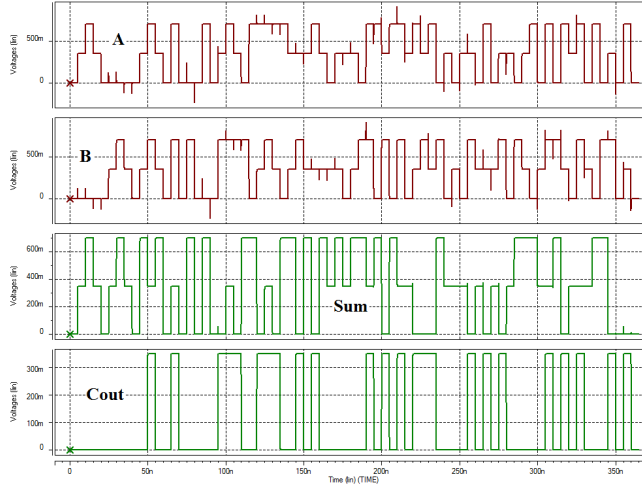


Figure 7. The waveforms of the proposed ternary half adder

Simulation results are shown in Table 4. The given structure operates faster in all power supply voltages due to its shorter critical path and higher driving capability. Although it consumes more power, the overall performance is even higher in 0.7V and 0.75V power supplies. The proposed design not only is a bit more efficient than the one presented in [7], but also benefits from 86 fewer transistors.

To put driving capability under test, load capacitors ranged from 2fF up to 10fF for both outputs are applied. The results of this experiment are illustrated in Fig. 8, which demonstrate the superiority of the proposed design. It charges and discharges the load capacitors much faster. As the output loads increase, the proposed design operates far more efficiently.

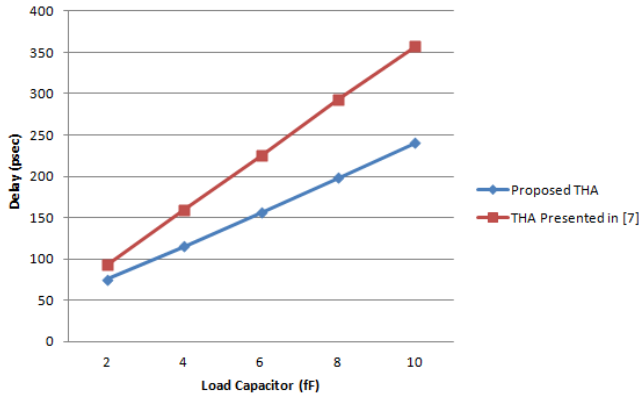


Figure 8. Delay vs. Load Capacitors

TABLE IV. SIMULATION RESULTS OF THE TERNARY HALF ADDERS

THA Cells	Delay (psec)	Power (μ W)	PDP (fJ)
$V_{dd} = 0.75V$			
Proposed THA	73.737	24.138	1.7799
THA presented in [7]	83.052	21.465	1.7827
$V_{dd} = 0.7V$			
Proposed THA	75.219	18.837	1.4169
THA presented in [7]	92.930	16.261	1.5112
$V_{dd} = 0.65V$			
Proposed THA	90.790	14.583	1.3240
THA presented in [7]	105.44	12.340	1.3011

IV. THE PROPOSED FULL ADDER

The proposed ternary half adder is cascaded twice to create a ternary full adder cell, the functionality of which is shown in Table 5. The new methodology is utilized to design carry generator circuit, which takes Cout1 and Cout2 as inputs. The output carry of the ternary half adder never becomes '2' (Table 1). Therefore, the highest boundary of 'Cout1+Cout2' is two (Table 6). The proposed ternary full adder is depicted in Fig. 9. It has 64 transistors. The waveforms are also depicted in Fig. 10.

TABLE V. THE TRUTH TABLE OF A TERNARY FULL ADDER

Σ_{in}	Cout	Sum
0	0	0
1	0	1
2	0	2
3	1	0
4	1	1
5	1	2
6	2	0

TABLE VI. THE TRUTH TABLE OF THE CARRY GENERATOR CIRCUIT AND ST PARAMETERS

Cout1	Cout2	Cout1 + Cout2	$\frac{Cout1 + Cout2}{2}$	ST	Cout
0	0	0	0	0.25	2
0	1	1	0.5		1
1	0	1	0.5	0.75	1
1	1	2	1		0

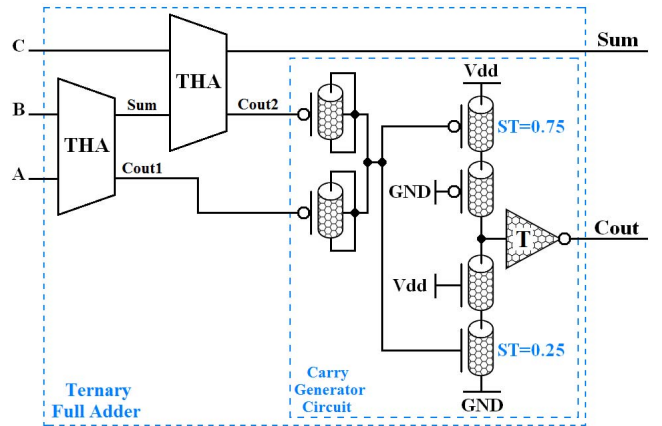


Figure 9. The proposed ternary full adder

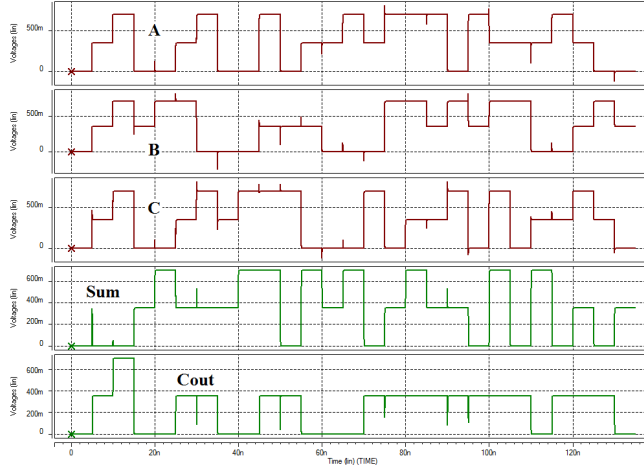


Figure 10. The waveforms of the proposed ternary full adder

The proposed ternary full adder and the design presented in [9] are simulated at the same conditions described in section 3. The results are shown in Table 7. The given structure outperforms the previously presented architecture in all power supply voltages. For example in 0.7V power supply, it operates 66% faster, and its PDP is 45% lower. In addition, it forms the entire cell with 42 fewer transistors.

V. 4-BIT TERNARY ADDER BLOCK

Finally, a 4-bit ternary ripple adder (Fig. 11) is constructed with the usage of new THA and TFA cells. THA presented in [7] together with TFA presented in [9] are also combined to form a hybrid 4-bit adder block. A worst case propagation delay input pattern for a 4-bit ternary ripple adder is fed, where one of the input operands changes from "0000" to "0001", while the other operand is "2222". It causes a change in the output from "02222" to "10000". The delay parameter when the new adder cells are used is 176.53psec. It takes 188.25psec for the hybrid approach to produce the final result.

VI. CONCLUSION

A novel ternary half adder cell has been proposed in this paper. Four progressive modifications have been carried out to reach the final design. It outshines the previously presented half adder in terms of delay and PDP. It also benefits from high driving power. In addition, transistor count has been reduced dramatically. Larger adder blocks such as a ternary full adder and a 4-bit adder block have also been formed with the use of proposed THA. The larger blocks also operate very efficiently.

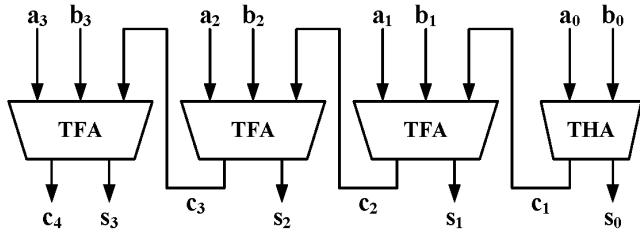


Figure 11 4-bit ternary ripple adder

TABLE VII. SIMULATION RESULTS OF THE TERNARY FULL ADDERS

TFA Cells	Delay (psec)	Power (μ W)	PDP (fJ)
$V_{dd} = 0.75V$			
Proposed TFA	96.413	49.243	4.7476
TFA presented in [9]	272.97	30.691	8.3777
$V_{dd} = 0.7V$			
Proposed TFA	107.70	38.069	4.1000
TFA presented in [9]	319.00	23.617	7.5338
$V_{dd} = 0.65V$			
Proposed TFA	134.03	28.752	3.8536
TFA presented in [9]	382.13	16.771	6.4087

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