



SDI Review Form 1.6

Journal Name:	<u>British Journal of Applied Science & Technology</u>
Manuscript Number:	2015_BJAST_18607
Title of the Manuscript:	Hardware Efficient Scheme for Indoor Environment Using Grid Mapping
Type of the Article	Original Research Article

General guideline for Peer Review process:

This journal's peer review policy states that **NO** manuscript should be rejected only on the basis of '**lack of Novelty**', provided the manuscript is scientifically robust and technically sound.

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PART 1: Review Comments

	Reviewer's comment	Author's comment (if agreed with reviewer, correct the manuscript and highlight that part in the manuscript. It is mandatory that authors should write his/her feedback here)
<u>Compulsory</u> REVISION comments	The article is devoted to the FPGA hardware implementation of path planning of the robot. Implemented in FPGA computation of the shortest path of the robot. An algorithm described, which is simple and known. Practically implemented information processing unit from the sensors and calculating control signals for guiding the movement of the robot. The authors show the results of test simulations for each block in the form of time diagrams. The analysis executed by the coverage area of FPGA, and by power consumption. However, have comments: 1. There is no a full description of the circuit of the unit in Fig. 3. Conditional blocks must have two outs, "yes" and "no". In figure are not at all conditional blocks have two outs. 2. Functioning of each block is represented as a waveform. However, the project is not described as a circuit or part of the behavioral model (for example, VHDL, Verilog). 3. On the diagram (Fig. 12) is not shown any units that represented consumption. 4. The paper shows the analysis of known algorithms, but not showed different variants of hardware implementation. Since the work is aimed at a known hardware implementation of the algorithm on FPGA, then you need show advantages in comparison with other hardware.	Comment 1: We changed the fig 3 (flow chart), modified in and outs of the figure. Comment 2: We changed the explanation of VLSI architectures with a behavioural model in section 3. Comment 3: The figure 11 units are represented in the form of CLB's (configuration logic blocks) occupancy Comment 4: Comparison results are mentioned in section 4.3 The other authors are not shown the device utilization of the their defined environment. The speed and time, distance is proportionatly changed with respect to the environment size.
<u>Minor</u> REVISION comments		
<u>Optional/General</u> comments		