

COMPARISON BETWEEN SPARTAN-3E AND VIRTEX-6 TECHNOLOGIES ON FPGA FOR UART TRANSMISSION

Abstract

This paper presents the hardware implementation of high speed and power efficient (Universal Asynchronous Receiver/Transmitter) UART using (Field Programmable Gate Array) FPGA. UART is an integrated circuit containing a transmitter (parallel to serial converter) and a receiver (serial to parallel converter) each clocked separately. It transmit 9600 to 34800 bps for transmitting data bit. A low power, high speed UART using different architectures and technologies has been designed. The design has been formulated at different technologies (90 nm and 40 nm) on FPGA's such as Spartan 3E and Virtex 6 synthesized on the xilinx ISE 12.4i in VHDL language. Results have been compared with different types of technologies.

Keywords— UART, FPGA, VHDL, XILINX ISE, LUT's, CLBs.

1 Introduction

An UART is a silicon microchip with programming that controls a computer's interface to its attached serial devices. Specifically, it provides the computer with the RS-232C DTE interface so that it can talk to and exchange data with modems and other serial devices (Conway and Dehaan, 2011). The UART consists of a transmitter, a baud rate generator and a receiver (Sharma and Gupta, 2009).

The rate at which the data is transmitted is known as Baud rate (Joshi et al, 2011). UART is mainly used because of its high speed, low power consumption, lesser cost and more fidelity as compared to ASICs. There are two primary forms of serial communication: synchronous and asynchronous. Synchronous serial transmission requires that the sender and receiver share a clock with one another, or that the sender provide a strobe or other timing signal so that the receiver knows when to "read" the next bit of the data. In most form of serial synchronous communication, if there is no data available at a given instant to transmit, a fill character must be sent instead so that data is always being transmitted. Asynchronous transmission allows data to be transmitted without the sender having to send a clock signal to the receiver (Kaur and Kaur, 2012). Asynchronous serial communication because of less transmission line, high reliability, and long transmission distance is usually implemented by UART (Yuan F. and Xue C., 2011). VHDL has been used to implement core functions of UART and integrate them into a FPGA chip. As we are using Finite State Machine for transmitter due to which our design has become less complex and the proposed UART becomes more stable, reliable and compact for serial data transmission (Wakhle, 2012). Due to which, the consumption of LUT's, flip-flops or in short the area consumption of the chip becomes less. We have also tested our design for the errors which arises during transmission of data to analyze that our output is free from the errors.

2. Methodology

VHDL code for UART transmitter is designed. VHDL programs have been implemented and tested on XILINX project Navigator Release 12.4i. Device utilization of higher (40nm) and lower (90nm) technology is taken. Timing summary of both technologies is taken. The performance of modified UART transmitter is evaluated by giving the tight timing constraints which provide better results then corresponding section at lower technology. The power performance of purposed technique has been evaluated with the use of XILINX power analyzer in terms of decipted power during ON condition and is compared with the performance of transmitter section at lower technology. Figure 1 shows the flow chart of UART transmitter and explains the functionality of transmitter that how data has been transmitted.

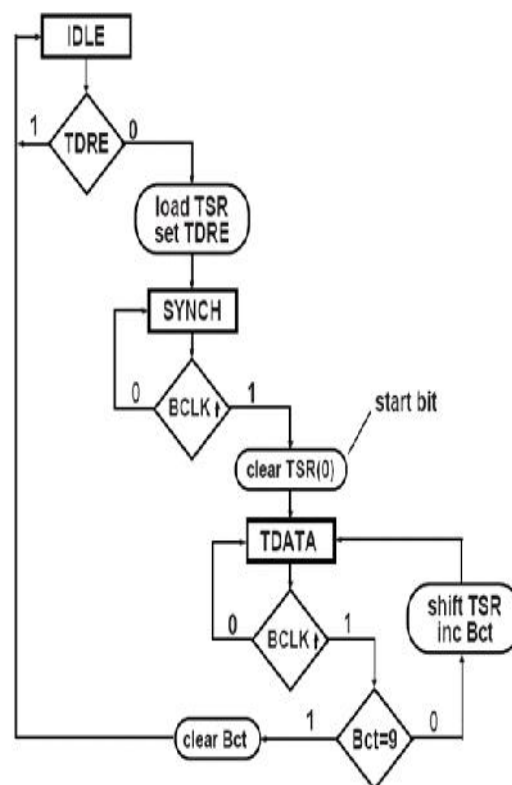


Figure 1: Flow Chart of UART Transmitter

3 Results

After implementation of VHDL code, figure 2 shows the Block diagram of UART Transmitter. Figure 3 and 4 show the RTL and Technology Schematic generated by the tool. RTL Schematic shows basic gates (like and, or, nand, nor, not etc), combinational circuits (like mux etc) and sequential circuits (flip-flops). Technology Schematic shows basic blocks i.e. configurable logic blocks (CLBs of FPGA). The CLBs of FPGA consist of look up tables LUT, buffer, mux and flip-flop. CLBs are the programmable logic components of FPGA. A logic block consists of a few logical cells called slices. CLBs are surrounded by a powerful hierarchy of versatile routing resources. FPGA manufacturers try to provide just enough tracks so that most designs that will fit in terms of LUTs and IOs can be routed. Table 1 shows the comparison between research paper and purposed UART on the basis of number of slices, look up tables, GCLK's, slice flip-flops and maximum frequency used. As compared with reference paper results shown by

using virtex 4 technology, the results shown by using virtex 6 technology uses 12% less number of slices, 45% less number of look up tables and 8% less number of flip-flops. Table 2 shows the comparison of two different technologies i.e. lower technology (90nm-spartan3e) and higher technology (40nm-virtex6). While doing comparison we will find that our research shows great significance as our all the parameters are consuming less area and consumes less power to operate.

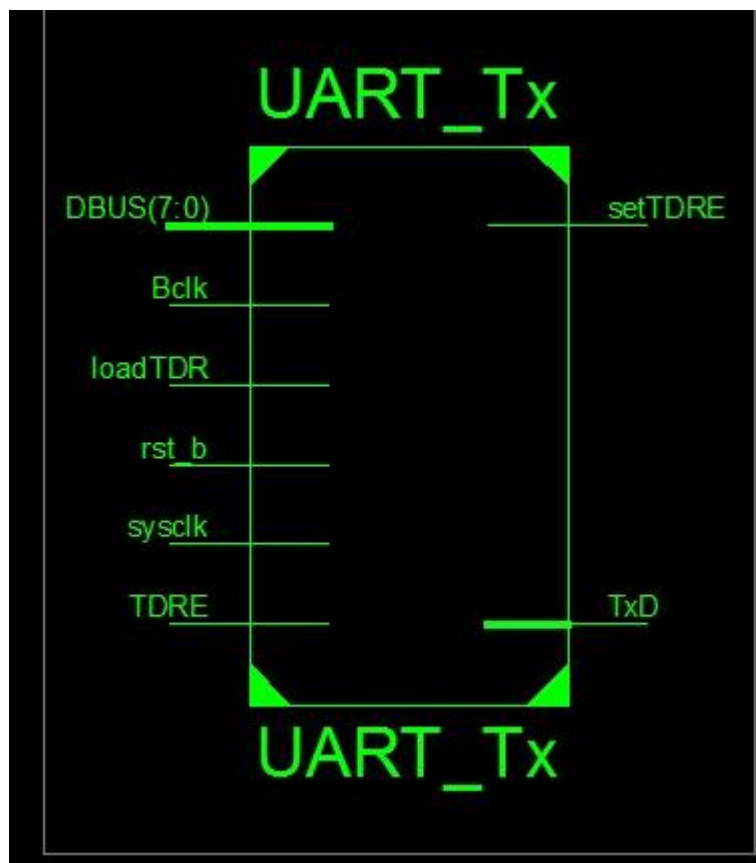


Figure 2: Block Diagram of UART Transmitter implemented in Xilinx ISE

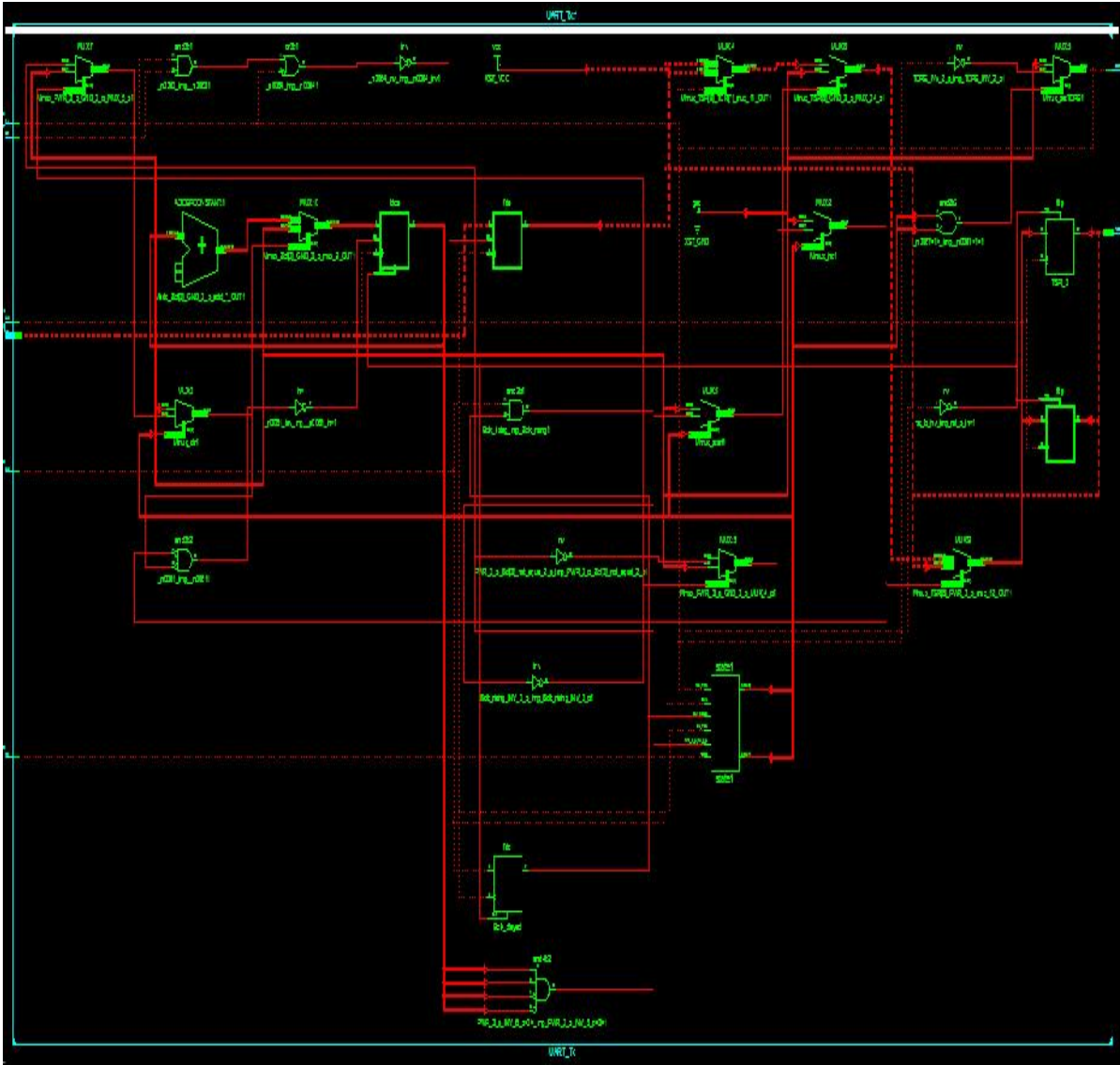


Figure 3: RTL Schematic of UART Transmitter

Table 1. Comparison between reference paper and proposed UART

S. No.	Parameters	Virtex4vfx 12sf363-10[4]	Virtex4vfx 12sf363-10	Virtex 3ff484	xc6vlx75t-
1	Number of slices	63	36	24	
2	LUTs	109	60	15	
3	GCLKs	2	1	1	
4	Slice flip flop	67	46	38	
5	Maximum frequency	289.151MHz	284.075MHz	735.998MHz	

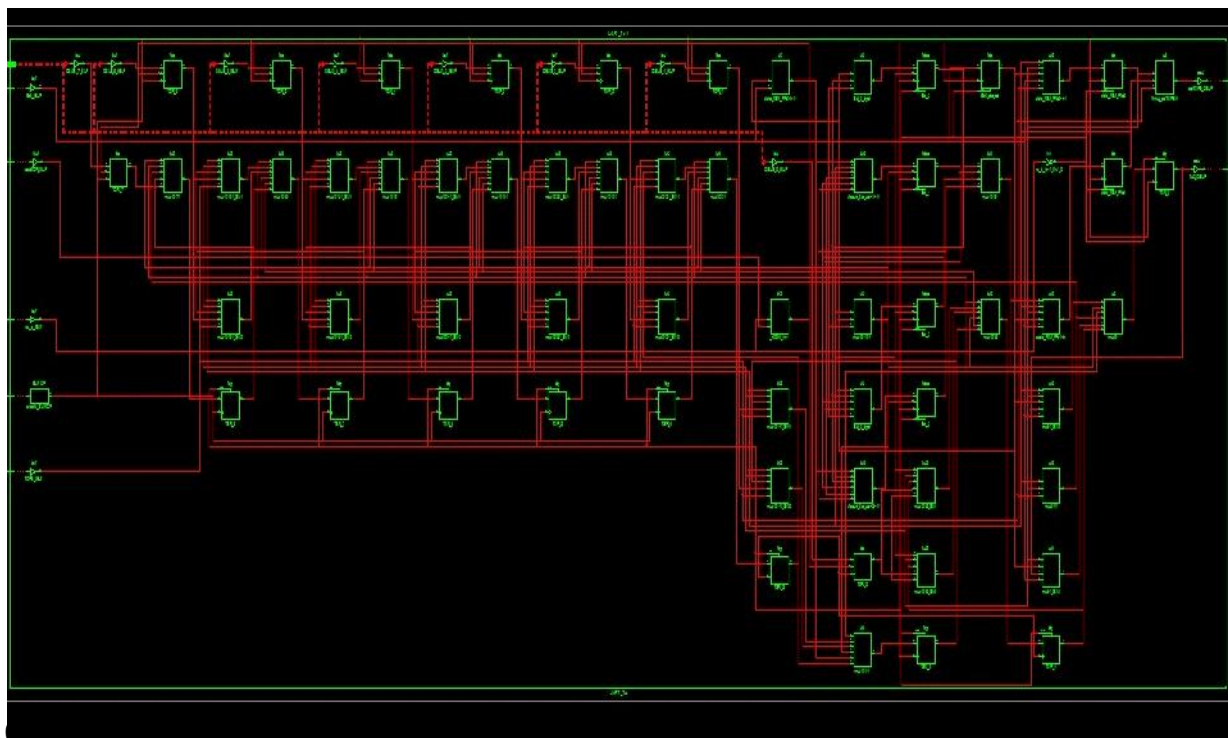


Figure 4: Technology Schematic of UART Transmitter

Table 2 Comparison between Spartan and Virtex technologies

Category	Spartan Technology	Virtex Technology
Target Device	XC3S100E-5VQ100	XC6VLX75T-3FF484
Technology	90 nm	40 nm
Number of slices	1% (18/960)	0% (24/93120)
Number of slice FF'S	1% (24/1920)	0% (38/46560)
Number of 4 I/P LUT'S	1% (26/1920)	31% (15/47)
Number of bonded IOBs	22% (15/66)	6% (15/240)
Number of GCLKs	4% (1/24)	3% (1/32)
Maximum Frequency	198.098MHZ	735.998MHZ

4 Conclusions

In this paper, we have discussed various methods to design UART. We examined different ways of designing and using different methods and concluded that use of higher technologies with improved architecture can enhance the speed of UART by 4 times. This implementation uses Verilog description language to get the modules of UART. After studying the comparative analysis, we conclude that there is a difference in between the number of slices, slice FF's, LUT's, IOB's, and GCLCK's. The results are quiet stable and reliable which provides the high bps rate.

References

- [1] Wakhle G.B. and Gaba I. (2012), "Synthesis and Implementation of UART using VHDL codes", pp. 1-3.
- [2] Kaur A and Kaur A. (2012), "An approach for designing a UART", vol.2, Issue 3, pp. 2305-2311.
- [3] Chakraborty A, Surbhi, Gupta S, Deshkar S and Jaisal P. k. (2012), "Design of Universal Asynchronous Receiver Transmitter Using VHDL", IJACST Vol. 3, Issue 1.
- [4] Wang Y and Song K. (2011), "A new approach to realize UART". pp. 2749-2752.
- [5] Yuan F. and Xue C. (2011), "Design and simulation of UART Serial Communication Module based upon VHDL".
- [6] Spartan-3E Starter kit Board User Guide. UG230-Xilinx, v.1.2, January 11, 2011 available at http://www.xilinx.com/support/documentation/boards_and_kits
- [7] Sharma P and Gupta A. (2009), "The IUP Journal of Science and technology", Vol: 5, No. 4, pp. 21-30.
- [8] Joshi K., Patel D., Patel C. and Kher R. (2011), "Design and simulation of UART IP core for FPGA implementation".
- [9] Kolte V.S (2012), "VLSI Design and Technology".Techmax Publicatios, pune-411009. pp. 48-49.
- [10] Norhuzaimin J and Maimun H.H. (2005), "The Design of High Speed UART", Asia-Pacific Conference on applied Electromagnetics.
- [11] L.K Hue and Q.CH.Wang (2006), "UART-based Reliable Communication and performance Analysis", Vol No.10, May 2006, pp. 15-21.