SDI Review Form 1.6

Journal Name:	**British Journal of Mathematics & Computer Science**
Manuscript Number:	**2013_BJMCS_7539**
Title of the Manuscript:	**COMPARISON BETWEEN SPARTAN-3E AND VIRTEX-6 TECHNOLOGIES ON FPGA FOR UART TRANSMISSION**
Type of the Article	**Computer Engineering**

General guideline for Peer Review process:

This journal's peer review policy states that **NO** manuscript should be rejected only on the basis of '**lack of Novelty**', provided the manuscript is scientifically robust and technically sound.
To know the complete guideline for Peer Review process, reviewers are requested to visit this link:

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PART 1: Review Comments

	Reviewer's comment	**Author's comment** *(if agreed with reviewer, correct the manuscript and highlight that part in the manuscript. It is mandatory that authors should write his/her feedback here)*
Compulsory REVISION comments	**1) Lines 49-51: the statement "Figure 1 shows the flow chart of UART transmitter and explains the functionality of transmitter that how data has been transmitted." , transmitter functionality explanations are not stated. In addition, all parts of the flow-chart in Figure 1 should be explained with their functionalities. "How can data be transmitted using such UART" should also be described.** **2) In Line 75: The statement "consumes less power to operate" should be proved.** **3) More explanations about Tables 1 and 2 are needed.** **4) In Line 110: the statement "In this paper, we have discussed various methods to design UART." is not right since various methods to design UART are not discussed.** **5) Lines 115&116: the statement "The results are quiet stable and reliable" is incorrect since the stability and the reliability of the system have not been Previously tested.** **6) In the list of References, journal titles for most references should be defined with specifications.**	
Minor REVISION comments	**1) Some Linguistic corrections are needed; such as In Line 7: "compared with different ..." should be**	

	corrected to "compared for different ...". **In Line 13: "An UART" should be corrected to " A UART".** **In Line 31: "a FPGA" should be corrected to " an FPGA"** **In Line 43: "technology" should be corrected to "technologies"** **In Line 46: "then corresponding" should be corrected to "than the corresponding"** **In Line 67: "the comparison between research paper" should be corrected to "the comparison between the results of a recent research in [4]"** **In Line 69: "As compared with reference paper results" should be corrected to "As compared with reference [4] results"** **In Line 74: "our research shows great significance as our all the parameters" should be corrected to "our research shows great significance as all parameters"** **Lines 110-116: The language of the section of Conclusions should also be improved.** **2) Lines 61-67: The descriptive statements "Technology Schematic shows basic blocks i.e. configurable logic blocks (CLBs of FPGA). The CLBs of FPGA consist of look up tables LUT, buffer, mux and flip-flop. CLBs are the programmable logic components of FPGA. A logic block consists of a few logical cells called slices. CLBs are surrounded by a powerful hierarchy of versatile routing resources. FPGA manufacturers try to provide just enough tracks so that most designs that will fit in terms of LUTs and IOs can be routed." do not belong to the Results of the paper and can rather be argued in the section of Introduction.**	

Optional/General comments	**It is better to change the title of the manuscript to " COMPARISON BETWEEN SPARTAN-3E AND VIRTEX-6 FPGA TECHNOLOGIES FOR UART TRANSMISSION" This manuscript proves the superiority of the (40nm-virtex6) technology in implementing the UART.**	

Note: Anonymous Reviewer