

Original Research Article

**A Proposed Modified Constant Frequency
Variable Duty PWM Based Speed Control
Technique for DC Motor Drives: A New Method
to Achieve More Precise Control over Speed**

ABSTRACT

In this paper, the authors have proposed a new method for speed control of DC motor drives via modified constant frequency-variable duty (CFVD) pulse width modulation (PWM) technique. An extra control signal is subtracted from the conventional fixed amplitude CFVD PWM signal to obtain the modified speed control signal. The peak amplitude of the subtracted extra control signal provides an additional control over the speed of DC motor along with the duty cycle of the ordinary PWM signal. A circuit for generating the modified control signal has been designed and fabricated. Finally the experiments are carried out to study the speed controlling characteristics of a 9 V DC motor drive. More precise control over speed, better transient response and abrupt electrical breaking of the motor have been achieved by using the proposed speed control signal as compared to the conventional CFVD PWM speed control signal.

Keywords: Pulse width modulation; DC motor, chopper control; duty cycle; modified CFVD PWM; electronic breaking; transient response.

1. INTRODUCTION

Pulse width modulation (PWM) which is synonymous with pulse duration modulation (PDM) is a commonly used technique for the speed of DC motor drives [1-4]. The average value of the voltage and current fed to the DC motor can be controlled by turning an electronic switch between the supply and motor on and off at a fast pace. Longer the switch is on as compared to the off periods, higher the power delivered to the motor. Since the speed (in rpm) of a DC motor is directly proportional to the average power delivered to it, thus by varying the supplied average power by means of variable on time period of the electronic switch, the speed of the DC motor can be controlled. The term 'duty cycle' is the ratio of the on time to the regular interval to the total time period. A low duty cycle corresponds to low power, since the supplied power is off for most of the time and vice versa. The PWM switching frequency has to be much faster than the response time of an electromechanical load such as DC motor drives. Typically from a few KHz to tens of KHz switching speed is used to control the speed of a variable speed DC motor drive [5]. The primary advantage of PWM based speed control is that, the power loss in the switching devices is almost negligible. When a switch is off, then there is practically no current through it and when the switch is on, then there is almost no voltage drop across it. Power loss, being the product of voltage and current, is thus zero in both the abovementioned cases.

PWM based speed control techniques are also sometimes called chopper control which are more power efficient, less complicated and less bulky as compared to the ordinary rheostat based speed control mechanisms of DC motor drives. Generally there are two different types

of PWM techniques may be used to control the speed of DC drives [6], such as (a) variable frequency-constant duty (VFCD) PWM and (b) constant frequency-variable duty (CFVD) PWM. In the first method, the frequency of the controlling signal may be varied keeping the duty cycle fixed (say at 50%) to vary the average voltage across the DC motor drive. And in the second case, the duty cycle is varied keeping the frequency of the controlling signal fixed to vary the average voltage across the DC motor drive. The second technique requires less complex circuitry to achieve wide range of variations in speed of the DC motors, which intern makes the entire system more cost effective. But the primary disadvantage of the conventional CFVD PWM technique is large abrupt mechanical shocks (kicks) have to be accepted by the rotating armature of a DC motor due to the application of large amplitude narrow pulse trains to achieve very low speed. This fact may result damage to the rotating mechanism of the armature which intern may reduce the life of the DC motor drive. Moreover the transient response the rotating drives are poor due to the presence of only a single controlling parameter, i.e. duty cycle of the PWM signal and absence of any other control to minimize the time required to increase or decrease the speed of the drive within any specified range. In this paper, the authors have proposed a new method for speed control of DC motors by modifying the conventional CFVD PWM technique via another extra control signal of special form. The extra control signal is subtracted from the conventional fixed amplitude CFVD PWM speed control signal to obtain the modified speed control signal. The peak amplitude of the extra control signal provides an additional control over the speed of DC motor along with the duty cycle of the ordinary PWM signal. A circuit for generating the modified control signal has been designed and fabricated. Finally the experiments are carried out to study the speed control characteristics of a 9 V DC motor by using the proposed method and those are compared with the characteristics obtained from ordinary CFVD PWM control technique. More precise control over speed, better transient response and abrupt electrical breaking of the DC motor drive are achieved by using the proposed method.

The rest of the paper is organized as follows. The next section describes the theoretical background associated with the conventional CFVD PWM based speed control technique in brief along with the proposed technique in detail. The design and fabrication methodologies of the proposed circuit to generate modified PWM signal are discussed in the section 3. The results obtained from the experiments are presented and discussed in the section 4. Finally the paper is concluded in the section 5.

2. THEORY

In this section, initially the conventional method of ordinary CFVD PWM technique for speed control of DC motor drives is discussed in brief. The disadvantages associated with the conventional method are also mentioned. Finally, the proposed method of DC motor speed control via modified CFVD PWM is discussed in detail.

2.1. Conventional CFVD PWM Speed Control Technique

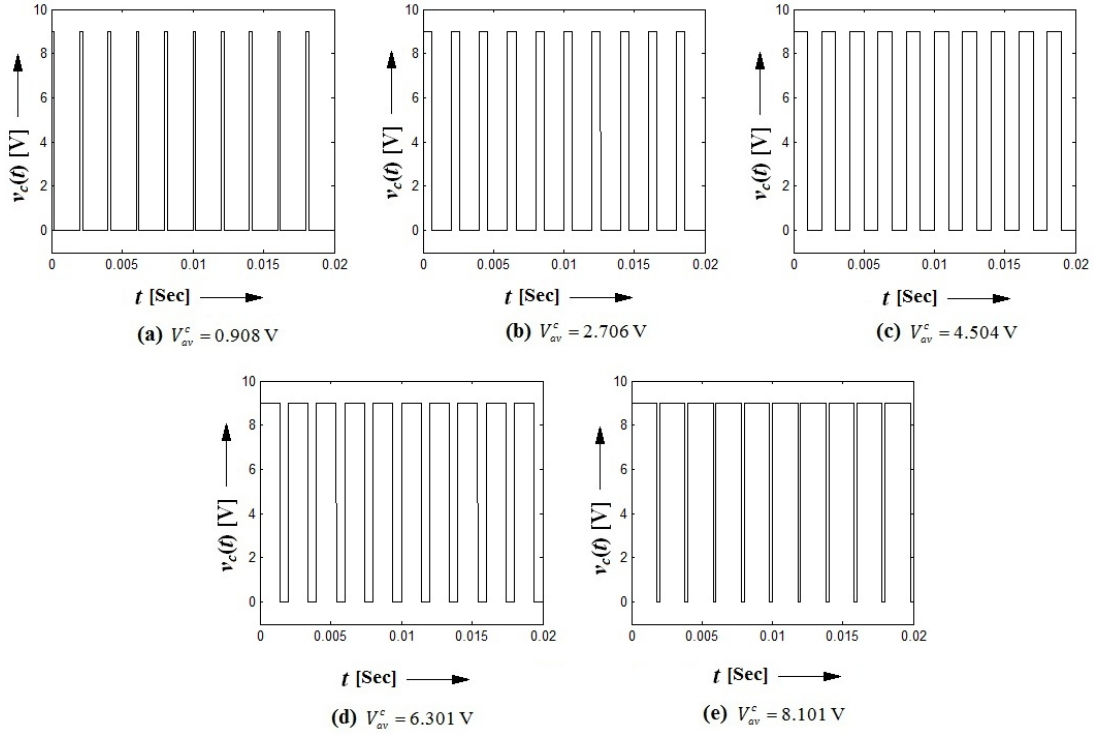
The typical CFVD PWM control signals of constant time period T_c (constant frequency $f_c = 1/T_c$) and peak amplitude V_c are shown in Figure 1 for different duty cycles ($d_c = T_{on}/T_c$; where $T_c = T_{on} + T_{off}$) such as (a) 10%, (b) 30%, (c) 50%, (d) 70% and (e) 90%. Mathematically the conventional CFVD PWM control signal may be expressed as

$$v_c(t) = \begin{cases} V_c & \text{for } iT_c < t \leq (d_c T_c + iT_c) \\ 0 & \text{for } (d_c T_c + iT_c) < t \leq (i+1)T_c \end{cases} \quad (1)$$

88 where $i = 0, 1, 2, 3, \dots$, etc. Now the average value of the control signal ($v_c(t)$) for duty
 89 cycle of d_c may be calculated as

$$90 \quad V_{av}^c = \frac{1}{T_c} \int_{iT_c}^{(i+1)T_c} v_c(t) dt = \frac{1}{T_c} \left[\int_{iT_c}^{(d_c T_c + iT_c)} V_c dt + \int_{(d_c T_c + iT_c)}^{(i+1)T_c} 0 dt \right] = d_c V_c. \quad (2)$$

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92

93 **Fig. 1. Typical conventional CFVD PWM control signals of frequency 500 Hz, peak**
 94 **amplitude 9 V for different duty cycles such as (a) 10%, (b) 30%, (c) 50%, (d) 70% and**
 95 **(e) 90%.**

96 Thus the average voltage V_{av}^c of the control signal ($v_c(t)$) is directly proportional to the duty
 97 cycle (d_c). By changing the value of d_c from 0 to 100%, the average voltage (V_{av}^c) can be
 98 changed from 0 to V_c . Speed of the DC motor (N in rpm) is directly proportional to V_{av}^c . Thus
 99 by varying the duty cycle of the control signal, the speed of the DC motor can be varied. But
 100 for constant V_c , the speed of the DC motor can only be varied within a single range by
 101 varying d_c . Very fast reduction or increase in speed is also cannot be achieved due to the
 102 inertia of the armature and absence of any additional control other than d_c . Moreover, due to
 103 application of train pulses of very small duty cycle ($d_c \leq 10\%$) to run the DC motor in very low
 104 rpm for long time, the rotating armature has to accept abrupt mechanical shocks (kicks)
 105 consecutively due to applied large amplitude narrow pulse trains, which may cause damage
 106 to the armature and consequently reducing the life of the DC motor.

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109 **2.2. The Proposed Technique**

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111 In the proposed method, a signal of form $v_s(t) = V_s(K_s - \sin(2\pi f_s t))$ (where $f_s = 1/T_s$ and T_s is
 112 the time period) of lower fundamental frequency (i.e. $f_s < f_c$; $\therefore T_s > T_c$) is subtracted from the
 113 conventional CFVD PWM speed control signal ($v_c(t)$) to obtain the modified control signal
 114 $v_{sc}(t) = v_c(t) - v_s(t)$. The fundamental frequency of the signal $v_s(t)$ is taken to be n -times
 115 smaller as compared to the fundamental frequency of $v_c(t)$ (i.e. $f_s = f_c/n$; $\therefore T_s = nT_c$, where n
 116 is an integer greater than one). The peak amplitude of the subtracted signal $v_s(t)$ (i.e. V_s)
 117 provides an additional control over speed of the DC motor along with the duty cycle (d_c) of
 118 the PWM control signal. The abovementioned modified PWM signals are shown in Figure 2
 119 for different duty cycles and for different V_s/V_c ratio. The mathematical expression of the
 120 overall control signal is given by

$$121 \quad v_{sc}(t) = \begin{cases} V_c - V_s \left[K_s - \sin\left(\frac{2\pi t}{nT_c} + \theta_{sc}\right) \right] & \text{for } iT_c < t \leq (d_c T_c + iT_c) \\ 0 & \text{for } (d_c T_c + iT_c) < t \leq (i+1)T_c \end{cases}, \quad (3)$$

122 where $i = 0, 1, 2, 3, \dots, (n-1)$; θ_{sc} is the initial phase of $v_s(t)$ and K_s is a constant
 123 associated with the circuit. The value of θ_{sc} may remain within the range $0 \leq \theta_{sc} \leq (2\pi/n)$.
 124 Now the average value of $v_{sc}(t)$ may be calculated as

$$125 \quad V_{av}^{sc} = \frac{1}{T_s} \int_0^{T_s} v_{sc}(t) dt = d_c (V_c - K_s V_s) + \frac{V_s}{nT_c} \sum_{i=0}^{(n-1)} \left(\int_{iT_c}^{(d_c T_c + iT_c)} \sin\left(\frac{2\pi t}{nT_c} + \theta_{sc}\right) dt \right). \quad (4)$$

126 The first term of equation (4) may be varied by varying either d_c or V_s or both simultaneously.
 127 The second term of the same equation is a function of d_c , V_s , n and θ_{sc} (say $\Theta(d_c, V_s, n, \theta_{sc})$).
 128 Thus by varying d_c , the average control voltage (V_{av}^{sc}) may be varied and consequently the
 129 speed of the DC motor may be varied. Moreover, for constant V_c , the peak amplitude of the
 130 subtracted signal $v_s(t)$ (i.e. V_s) provides an additional control over V_{av}^{sc} which intern leads to
 131 an additional control over the speed of the DC motor. The average voltage of the overall
 132 control signal (i.e. V_{av}^{sc}) becomes negative for

$$133 \quad \left(\frac{V_s}{V_c} \right) > \left(\frac{nd_c T_c}{nd_c K_s T_c - \Theta} \right) = \frac{1}{K_s} \quad (\because \Theta \ll nd_c K_s T_c \quad \forall d_c > 0). \quad (5)$$

134 Thus the direction of the rotation of the DC motor can be reversed by changing the V_s/V_c
 135 ratio above the specified value given in equation (5). Faster control over the speed reduction
 136 or increment, i.e. better transient characteristics can also be achieved due this additional
 137 control mechanism. Electrical braking of the DC motor can also be achieved by varying V_s
 138 for a particular d_c . Moreover, for smaller duty cycles ($d_c \leq 10\%$), due to gradual increment or
 139 decrement of the amplitudes of the consecutive narrow pulses, possibility of abrupt
 140 mechanical shocks on the armature rotating in lower speed may also be avoided, which
 141 intern leads to achieve longer life of DC motors.

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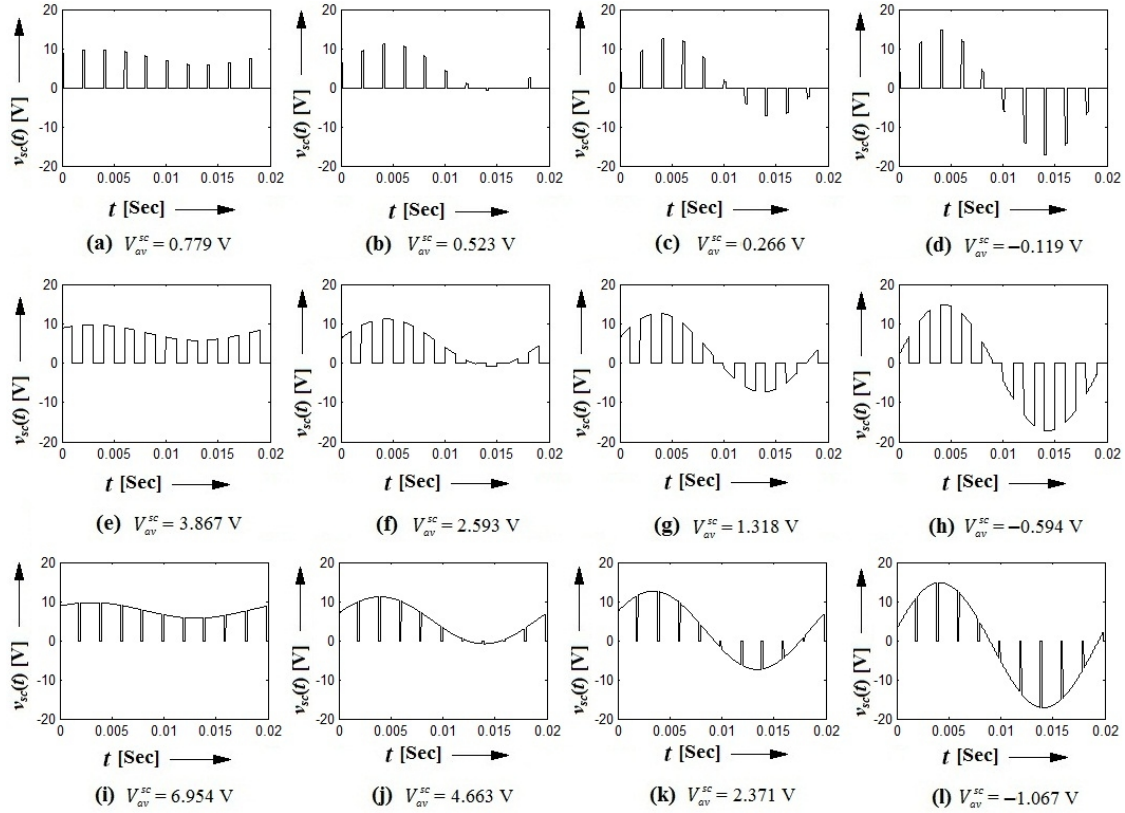


Fig. 2. Typical proposed modified PWM control signals (here $n = 10$); here the frequency and peak amplitude of the pulse train ($v_c(t)$) are taken to be $f_c = 500$ Hz and $V_c = 9$ V respectively; the duty cycles of the pulse train ($v_c(t)$) are taken to be 10% in (a) – (d), 50% in (e) – (h) and 90% in (i) – (l); the V_s/V_c ratio are taken to be 0.22 in (a), (e) and (i), 0.67 in (b), (f) and (j), 1.11 in (c), (g) and (k) and 1.78 in (d), (h) and (l).

3. DESIGN AND FABRICATION OF THE CIRCUIT

The block diagram of the system to generate the proposed modified PWM signal for speed control of DC drives is shown in Figure 3. At first a circuit capable of generating fixed amplitude CFVD PWM signal ($v_c(t)$) has been designed. The AC main supply voltage (230 V, 50 Hz) has to be stepped down via a centre-tapped step down transformer. Variable amplitude of the sinusoidal signal at the secondary of the transformer may be achieved via a potentiometer (POT) connected across the secondary terminals. The adjustable amplitude sinusoidal signal must be first rectified via a full-wave rectifier and then filtered by using a suitably designed low pass filter (LPF) to obtain the term $K_s V_s$ (where $K_s = 2/\pi$). An analog subtractor circuit may be used to obtain the difference between the terms $K_s V_s$ and $V_s \sin(2\pi f_s t)$, i.e. to construct the extra control signal $v_s(t)$. Finally another analog subtractor circuit may be used to obtain the proposed modified PWM control signal, i.e. $v_{sc}(t) = v_c(t) - v_s(t)$ as shown in Figure 3.

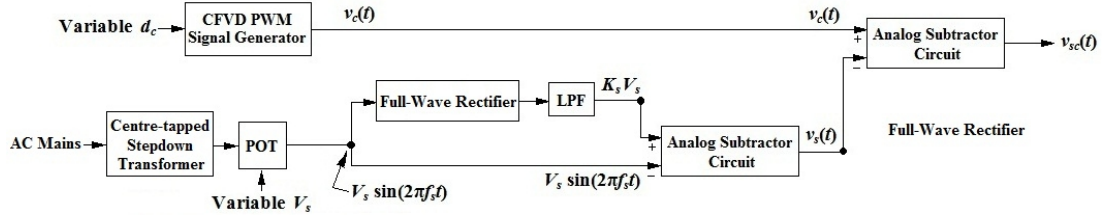


Fig. 3. Block diagram of the system to generate the proposed modified PWM signal.

The final designed circuit is shown in Figure 4. A 555 timer IC based astable multivibrator circuit is used to generate fixed amplitude CFVD PWM signal ($v_c(t)$). The output of this circuit (at pin 3) provides a square-wave of fixed amplitude $V_c = 9$ V and frequency $f_c = 483.09$. The duty cycle of the output square-wave may be varied by adjusting the 10 K Ω potentiometer (POT 1). Three 0.1 μ F ceramic disk capacitors are connected in parallel to obtain the desired value of the frequency determining capacitor, i.e. $C = 0.3$ μ F. Say, for a particular position of POT1, the left side of it, i.e. from wiper to the cathode of the diode D1 has the value R_a and similarly the right side of POT1, i.e. from the wiper to the anode of the diode D2 have the value R_b (obviously $R_a + R_b = 10$ K Ω), then the frequency determining capacitor, i.e. C will be charged from the 9 V DC supply through $R_1 = 500$ Ω resistor, diode D1 and finally R_a . The capacitor C will be charged up to $2/3$ of V_{cc} (i.e. up to 6 V). Thus the total charging time may be easily calculated as $T_{on} = 0.69(R_1 + R_{f1} + R_a)C$ [7], where R_{f1} is the forward resistance of the diode D1. After the complete charging up to $2V_{cc}/3$, the capacitor will discharge through the resistor R_b and diode D2. The discharging will occur until the voltage across the capacitor just falls below $V_{cc}/3$ (i.e. 3 V); after which again the charging will start through the previous path as mentioned earlier. The total discharging period may be calculated as $T_{off} = 0.69(R_b + R_{f2})C$ [7], where R_{f2} is the forward resistance of the diode D2. These charging and discharging processes will be continued repetitively. The time period of the output square-wave is given by $T_c = T_{on} + T_{off} = 0.69(R_1 + R_{f1} + R_{f2} + R_a + R_b)C$. Thus the expressions of frequency and the duty cycle may be written as $f_c = 1/T_c = 1/[0.69(R_1 + R_{f1} + R_{f2} + R_a + R_b)C]$ and $d_c = T_{on}/T_c = (R_1 + R_{f1} + R_a)/(R_1 + R_{f1} + R_{f2} + R_a + R_b)$. If the POT1 is adjusted then both the values of R_a and R_b will change simultaneously, but summation of them will remain always fixed, i.e. $R_a + R_b = 10$ K Ω . Thus by adjusting POT1, the duty cycle (d_c) will vary accordingly, but the frequency (f_c) will remain unchanged. Therefore the output waveform is the desired CFVD PWM control signal ($v_c(t)$) whose duty cycle (d_c) may be changed by adjusting the POT1 keeping the frequency of oscillation (f_c) unchanged.

A centre-tapped transformer (T) is used to step down the 230 V, 50 Hz AC main supply to 18 – 0 – 18 V, 50 Hz sinusoidal signal. A 10 K Ω potentiometer (POT2) is connected across the secondary terminals to obtain the adjustable AC voltage amplitude (V_s) at the secondary. A full-wave rectifier circuit comprising of two rectifying diodes (D3 and D4) cascaded with a shunt capacitor (1000 μ F) LPF is used to obtain the steady term $K_s V_s$ (here $K_s = 2/\pi$) which is fed at the non-inverting input of the analog subtractor circuit made of IC 741 operational amplifier (biased via $V_{CC} = +20$ V, $V_{EE} = -20$ V). The voltage across the POT2 (i.e. $V_s \sin(2\pi f_s t)$) is given as another input to the subtractor circuit at the inverting input terminal. Thus at the output of the will provide the desired extra control signal $v_s(t) = V_s(K_s - \sin(2\pi f_s t))$ with adjustable V_s via POT2, where $K_s = 2/\pi$ and $f_s = 50$ Hz. Initially the offset nullification of the Op-Amp has been achieved by adjusting the 10 K Ω POT3 as shown in Figure 4. Another similar analog subtractor circuit finally used to obtain the difference between $v_c(t)$ and $v_s(t)$ to construct the proposed modified CFVD PWM signal $v_{sc}(t) = v_c(t) - v_s(t)$. Finally a motor driver circuit made of CL 100 n - p - n BJT and 1 K Ω resistance is used to drive the 9 V DC motor via the proposed control signal ($v_{sc}(t)$) as shown in Figure 4.

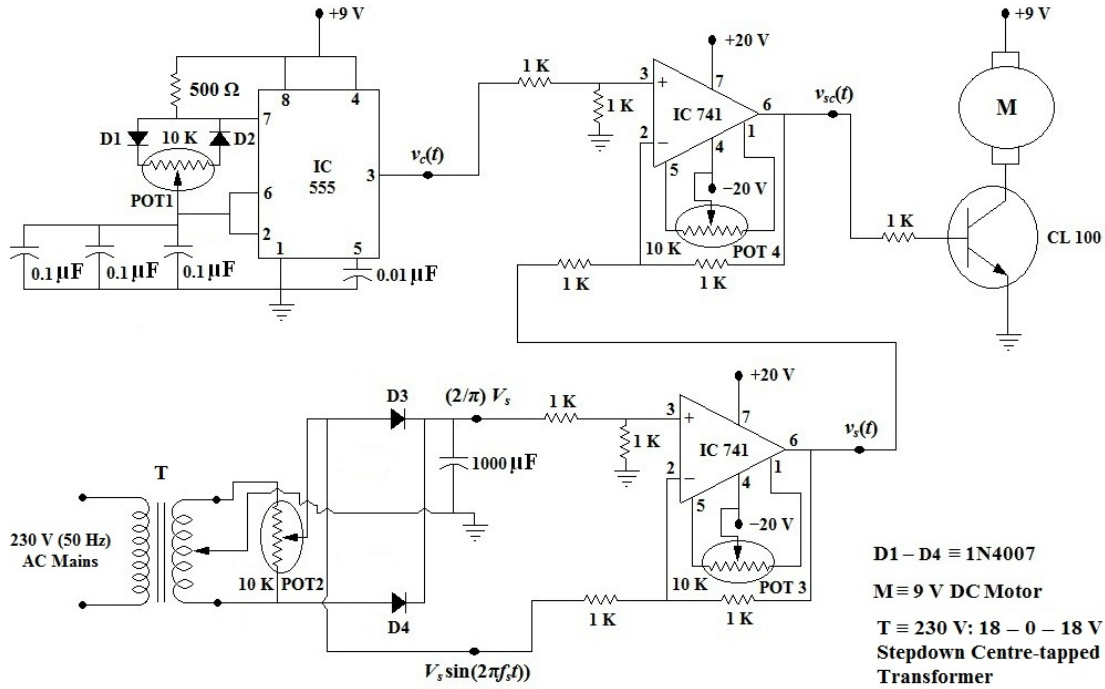


Fig. 4. The final designed circuit to generate the proposed modified PWM signal.

The complete PCB layout of the designed circuit has been sketched via “EAGLE 5.10.0 Light” software [8]. After obtaining the layouts, the said PCB has been fabricated via chemical etching procedure [9] and finally the components are carefully soldered on the fabricated PCB to obtain the complete module to carry out experimental measurements.

4. EXPERIMENTAL RESULTS AND DISCUSSION

After fabrication of the designed circuit described in the previous section, the experiments are carried out to study the speed control characteristics of a 9 V DC motor drive via the proposed method and results are compared with those obtained via the conventional CFVD PWM speed control technique. Initially the accuracy of performance of the fabricated circuit has been verified by measuring average voltages of the modified PWM signal (V_{av}^{sc}) at different duty cycles (d_c) of the PWM signal for different peak amplitudes of the extra control signal (V_s). At first the value of V_s has been set at a particular value (any one of 0, 2, 4, 6, 8, 10, 12, 14 and 16 V) by adjusting the POT2 and by observing the waveform of $V_s \sin(2\pi f_s t)$ at the input of the full-wave rectifier section in channel 1 of a digital storage oscilloscope (DSO) display. For particular value of V_s , the duty cycle of the (d_c) of the PWM signal has been varied from 5 – 95% in a step increment of 5% by adjusting the POT1 at each case and observing the PWM waveform at the pin 3 of IC 555 in channel 2 of the DSO display and for each and every value of d_c the average value of $v_{sc}(t)$ (i.e. V_{av}^{sc}) has been measured by using a DC voltmeter connected across the DC motor (not shown in Figure 4). Both the theoretically (equation (4)) and experimentally obtained variations of average voltage across the 9 V DC motor with duty cycle of the PWM signal for different values of peak amplitude of the extra control signal such as $V_s = 0$ V, $V_s = 2$ V, $V_s = 4$ V, $V_s = 6$ V, $V_s = 8$ V, $V_s = 10$ V, $V_s = 12$ V, $V_s = 14$ V and $V_s = 16$ V are shown in Figures 5 (a) – (i). It is interesting to observe

from Figures 5 (a) – (i), the theoretical and experimental results are close in agreement which intern proves that the accuracy of performance of the fabricated circuit is sufficient. It is also noteworthy that the values of V_{av}^{sc} become negative for all d_c (5 – 95%) while the value of V_s exceeds 14 V. This reversal of sign of V_{av}^{sc} due to $V_s > 14$ V indicates the change in the direction of rotation of the DC motor drive.

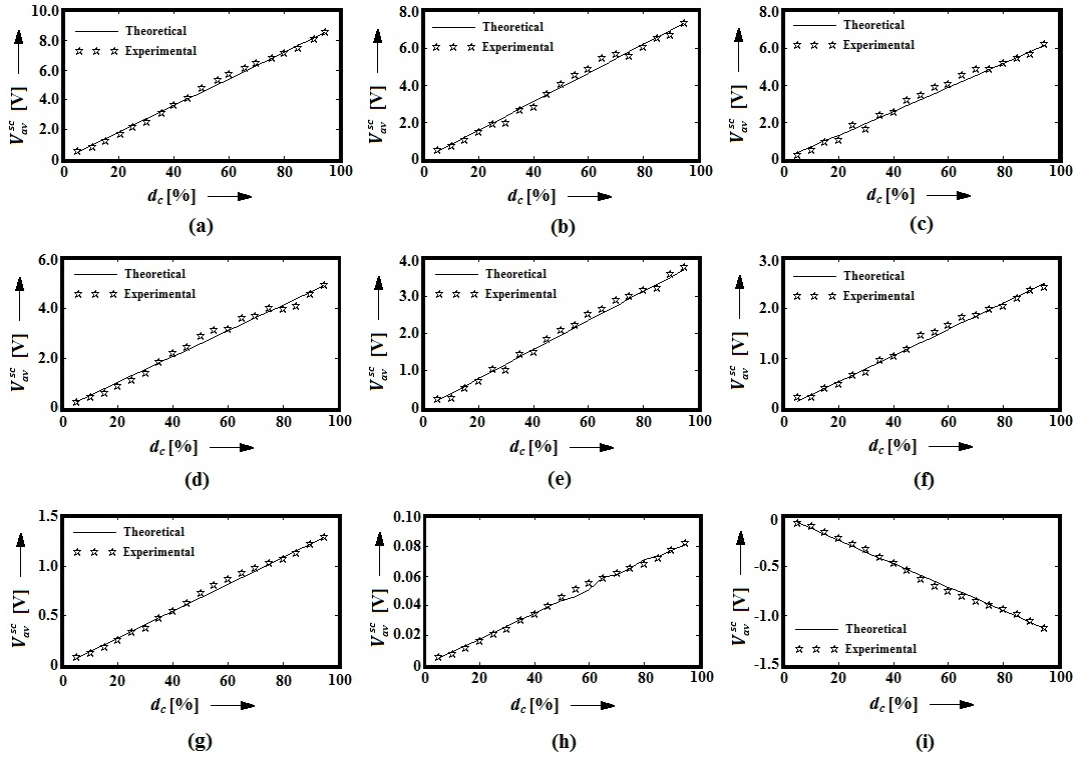


Fig. 5. Variations of applied average voltage across the 9 V DC motor with duty cycle of the PWM signal for different values of peak amplitude of the extra control signal such as (a) $V_s = 0$ V, (b) $V_s = 2$ V, (c) $V_s = 4$ V, (d) $V_s = 6$ V, (e) $V_s = 8$ V, (f) $V_s = 10$ V, (g) $V_s = 12$ V, (h) $V_s = 14$ V and (i) $V_s = 16$ V; here $f_c = 483.09$ Hz, $f_s = 50$ Hz and θ_{sc} is chosen to be any random value within the range $0 \leq \theta_{sc} \leq (2\pi/n)$ for each case of theoretical calculation.

The average current through the DC motor (I_{av0}^{sc}) under no load or free running condition for each and every average voltage across it (V_{av}^{sc}) have been measured by using a DC ammeter connected series with the DC motor drive (not shown in Figure 4). The variations of average current through the 9 V DC motor (I_{av0}^{sc}) under no load or free running condition with applied average voltage across it (V_{av}^{sc}) for different values of peak amplitude of the extra control signal such as $V_s = 0$ V, $V_s = 2$ V, $V_s = 4$ V, $V_s = 6$ V, $V_s = 8$ V, $V_s = 10$ V, $V_s = 12$ V, $V_s = 14$ V and $V_s = 16$ V are shown in Figures 6 (a) – (i). It is observe from Figures 6 (a) – (i) that for $V_s \leq 14$ V both the values of I_{av0}^{sc} and V_{av}^{sc} for all d_c values are found to be positive (i.e. quadrant (I) operation), but for $V_s > 14$ V both the values of I_{av0}^{sc} and V_{av}^{sc} for all d_c values

are found to be negative which indicates the quadrant (III) operation leading to reversal in direction of rotation.

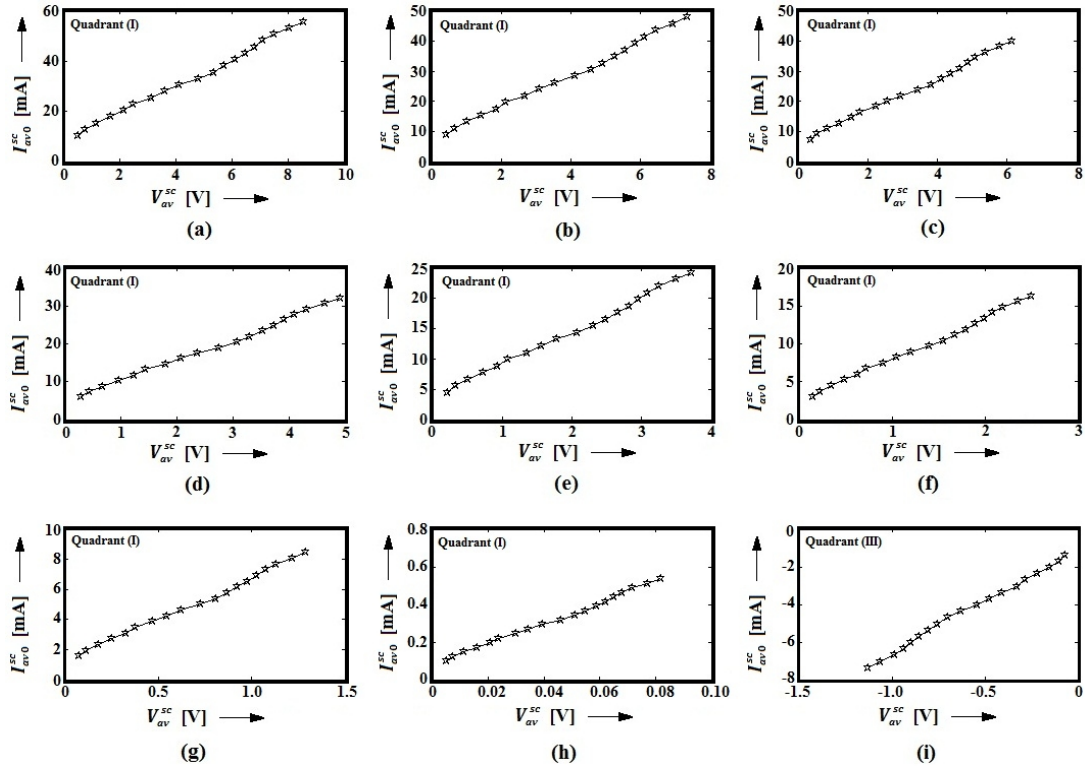


Fig. 6. Variations of average current through the 9 V DC motor under no load or free running condition with applied average voltage across it for different values of peak amplitude of the extra control signal such as (a) $V_s = 0$ V, (b) $V_s = 2$ V, (c) $V_s = 4$ V, (d) $V_s = 6$ V, (e) $V_s = 8$ V, (f) $V_s = 10$ V, (g) $V_s = 12$ V, (h) $V_s = 14$ V and (i) $V_s = 16$ V.

Variations of no load average current (I_{av0}^{sc}) through the 9 V DC motor drive and applied average voltage across it (V_{av}^{sc}) with peak amplitude of the extra control signal (V_s) for different duty cycles (d_c) of the PWM signal are shown in Figure 7. It is observed from Figure 7 that both the I_{av0}^{sc} and V_{av}^{sc} decrease with the increase of V_s for all values of d_c . It is interesting to note from Figure 7 that signs of both I_{av0}^{sc} and V_{av}^{sc} reversed from positive to negative while the value of V_s increased just above 14.137 V precisely; this value is exactly equal to the critical value of V_s obtained from equation (5) above which the sign reversal of both I_{av0}^{sc} and V_{av}^{sc} occur, i.e. $(V_s)_{critical} = \pi V_c / 2 = 14.137$ V (where $V_c = 9$ V).

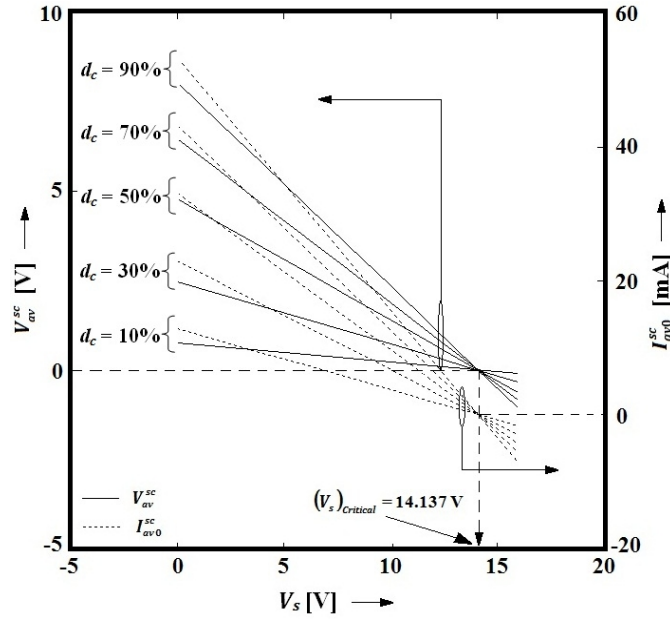


Fig. 7. Variations of no load average current through the 9 V DC motor and applied average voltage across it with peak amplitude of the extra control signal for different duty cycles of the PWM signal.

The speed of the 9V DC motor (N) in rpm under no load condition has been measured at different duty cycles (d_c) of the PWM signal for different peak amplitudes (V_s) of the extra control signal via a photo-contact tachometer (model DT-205L [10]). Photo-contact tachometer enables direct rpm measurements sensed from an easy to aim visible light beam directed toward a rotating shaft without mechanical contact; leading to more precise measurement of speed of the rotating shaft of the DC motor under no load or free running condition. Variations of speed of the DC motor under no load condition with duty cycles of the PWM signal for different peak amplitudes of the extra control signal and with peak amplitude of the extra control signal for different duty cycles of the PWM signal are shown in Figure 8. It is interesting to observe from Figure 8 (a) that the parameter V_s provides an extra control over speed along with the d_c . The range of the speed (in rpm) of the DC motor (i.e. starting from minimum speed (N_{min}) up to the maximum speed (N_{max})) may be selected by selecting the corresponding value of V_s (easily obtainable from Figure 8 (a)) and the speed of the DC drive may be varied from the selected N_{min} to N_{max} by varying the duty cycle (d_c) of the PWM control signal. Moreover, it is observed from Figure 8 (b) that the electronic breaking of the rotating DC motor drive rotating in any speed (i.e. for any fixed $d_c > 0$) may be achieved by abruptly changing the value of V_s just above critical value of it, i.e. $(V_s)_{critical} = 14.137$ V for which the speed of rotation will be either zero or its direction will be reversed.

Two types of electronic breaking characteristics of the 9 V DC motor drive are studies by abruptly varying V_s from 0 V to 14.137 V, keeping d_c fixed as well as by abruptly varying d_c from 90% to 10%, keeping V_s fixed and the results are given in Tables 1 and 2 respectively. For each of the abovementioned cases the time required for achieving the steady state minimum speed, i.e. breaking time (t_b) have been measured for five times via a precise online stopwatch [11] and finally average value of t_b has been calculated for each case. A comparative study of both the said electronic breaking methods from Table 1 and 2 reveals that the electronic breaking by abruptly varying V_s from 0 V to 14.137 V, keeping d_c fixed is more shaper and takes less breaking time as compared to its other counterpart.

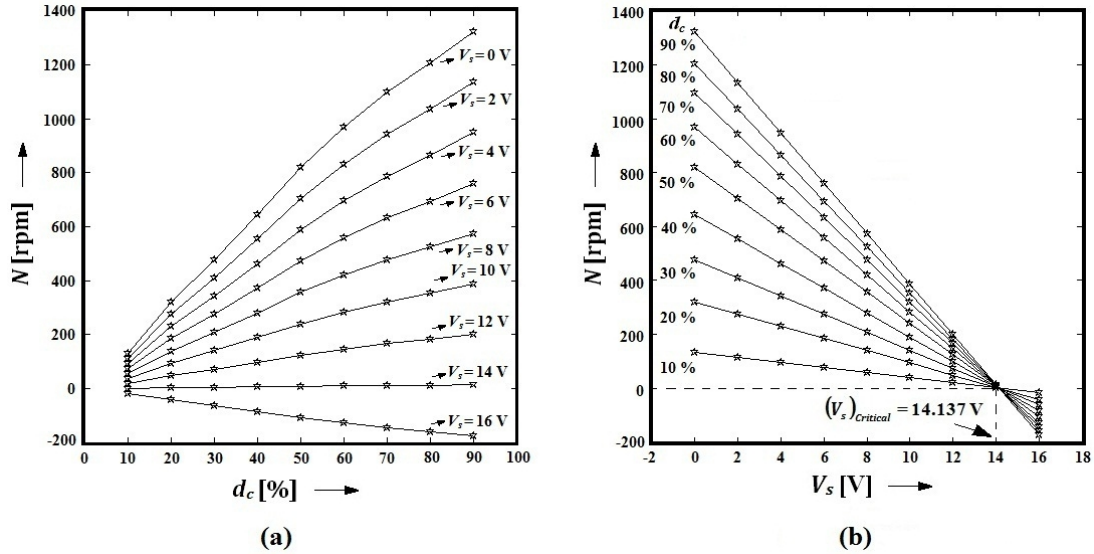


Fig. 8. Variations of speed of the DC motor under no load condition (a) with duty cycles of the PWM signal for different peak amplitudes of the extra control signal and (b) with peak amplitude of the extra control signal for different duty cycles of the PWM signal.

Table 1. Electronic breaking characteristics by abruptly varying V_s from 0 V to 14.137 V, keeping d_c fixed.

d_c (%)	N_{max} (rpm)	N_{min} (rpm)	t_b (ms)
90	1323.60	0	511
80	1207.00	0	497
70	1098.50	0	463
60	970.25	0	447
50	819.82	0	427
40	644.89	0	395
30	478.13	0	341
20	320.99	0	278
10	130.96	0	167

Table 2. Electronic breaking characteristics by abruptly varying d_c from 90% to 10%, keeping V_s fixed.

V_s (V)	N_{max} (rpm)	N_{min} (rpm)	t_b (ms)
0	1323.60	131.00	1059
2	1136.40	112.40	941
4	949.03	93.90	872
6	761.83	75.38	797
8	574.47	56.84	651
10	387.26	38.32	602
12	199.99	19.79	523
14	12.68	1.25	198
16	-174.51	-17.27	504

The transient speed control characteristics of the DC motor drive under test have been studied for different speed ranges such as 0 – 100, 100 – 300, 300 – 500, 500 – 700, 700 – 900, 900 – 1100 and 1100 – 1300 rpm. The settling times (t_s) have been measured via

precise online stopwatch [11] for each of the above mentioned ranges during both speed rise and decay by either varying d_c , keeping V_s fixed or varying V_s , keeping d_c fixed. Average settling time ($\hat{t}_s$) for each case has been calculated from five consecutive measurement data corresponding to that. It is noteworthy from Figures 9 (a) and (b) that average settling times ($\hat{t}_s$) for each of the ranges under consideration during both speed rise and decay are found to be smaller when the V_s is varied keeping d_c fixed as compared to when d_c is varied keeping V_s fixed. Thus the transient speed control characteristics via the extra control parameter V_s are found to be better as compared to the direct control parameter d_c .

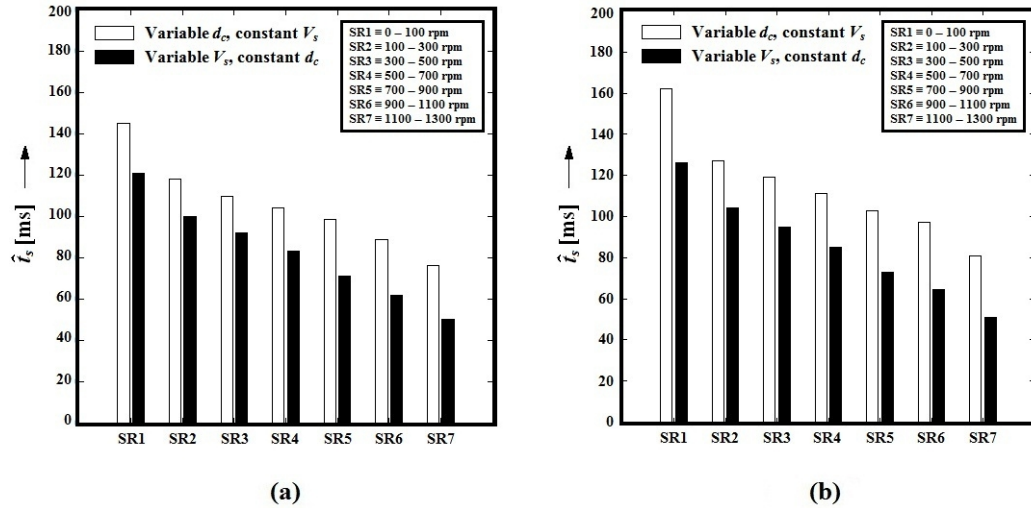


Fig. 9. Bar graphs showing the average settling times for different speed ranges when the duty cycle of the PWM signal is varied keeping the peak amplitude of the extra control signal fixed and when the peak amplitude of the extra control signal is varied keeping the duty cycle of the PWM signal fixed; (a) during speed rise, (b) during speed decay.

5. CONCLUSION

A new method for the speed control of DC motor drives via modified CFVD PWM technique has been proposed in this paper. An extra control signal having special form is subtracted from the conventional fixed amplitude CFVD PWM signal to obtain the modified speed control signal. The peak amplitude of the subtracted extra control signal provides an additional control over the speed of DC motor along with the duty cycle of the ordinary PWM signal. An electronic circuit for generating the modified control signal for 9 V DC motor drive has been designed and fabricated and the experiments are carried out to study the speed control characteristics of the DC motor under test. More precise control over speed, better transient response and abrupt electrical breaking of the motor have been achieved by using the proposed speed control signal as compared to the conventional CFVD PWM speed control signal.

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